IN THE CLAIMS

Please amend Claims 1 to 5 as shown below. The claims, as pending in the subject application, read as follows:

1. (Currently amended) A transfer ~~system~~ controller ~~in~~ which is connected to a plurality of CPUs ~~connected through a shared bus are connected to~~ and a plurality of memory devices ~~units~~ or IO devices, said controller ~~through a bus for separate transfer of a read instruction from a read data return,~~ comprising:

transfer means for transferring an instruction from a CPU to a destination device and for transferring read data from the destination device to the CPU when the instruction is a read instruction, the read data being transferred at time separate from the time of transferring the corresponding read instruction;

holding means for holding information associated with a CPU which issues a new instruction and information associated with a destination device of the new instruction, and for holding information associated with a CPU which issues an instruction ~~being~~ which is suspended and information associated with a destination device of the suspended instruction; and

order control means for controlling said transfer means to transfer a plurality of read ~~an issue order of return~~ data in accordance with an order of transferring the corresponding read instructions ~~and a transfer instruction~~ based on held contents of said holding means ~~in a read time; and~~

~~issue means for issuing transfers, which are first serialized and transferred through the shared bus, in parallel using a plurality of connection paths~~.

2. (Currently amended) The transfer ~~system~~ controller according to claim 1, wherein the plurality of CPUs are connected through a shared bus, said controller further comprising

means for queuing a transaction request output to the shared bus after bus snooping through the shared bus.

3. (Currently amended) The transfer ~~system~~ controller according to claim 1, wherein

said order control means comprises determination means for determining whether or not a transaction can be issued to a destination device in response to a read request based on the held contents of said holding means.

4. (Currently amended) The transfer ~~system~~ controller according to claim 3, wherein

said determination means determines that the transaction cannot be issued when a destination device of a new instruction is an IO device, and a transfer of an instruction to a different IO device is suspended.

5. (Currently amended) The transfer ~~system~~ controller according to claim 3, wherein

said determination means determines that the transaction cannot be issued when a destination device of a new instruction is a memory device, and a transfer of an instruction issued by a different CPU is suspended.